UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,224	11/19/2001	Christopher K. Sutton	10990531-1	5410

7590 06/04/2004

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 272400
Loveland, CO 80537-0599

EXAMINER
LAU, TUNG S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,224	SUTTON ET AL.	
	Examin r	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on th cover sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,15,16,18,19 and 21-24* is/are rejected.

7)☒ Claim(s) *6,13,14,17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 11, 21, 23, 2, 4, 5, 8, 9, 10, 16, 18, 15, 7, 19, 22, 24, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sutton (U.S. Patent Application 2003/0078679).

Regarding claim 1:

Sutton discloses an electronic test system for testing an electronic device under test (DUT), said test system comprising an electronic processor (fig. 1, unit 102); an electronic memory coupled to said electronic processor (fig. 1, unit 101); a hierarchical program structure residing in said memory and executed by said processor (page 2, section 0023-0025), said hierarchical program structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (page 2, section 0023-0025), to a test level corresponding to one or more of said measurements (page 2, section

0023-0025), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (page 2, section 0023-0025).

Regarding claim 3:

Sutton discloses an electronic test system for testing an electronic device under test (DUT), said test system comprising an electronic processor (fig. 1, unit 102); an electronic memory coupled to said electronic processor (fig. 1, unit 101); a hierarchical program structure residing in said memory and executed by said processor (page 2, section 0023-0025), said hierarchical program structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (page 2, section 0023-0025), a test level corresponding to one or more of said measurements (page 2, section 0023-0025), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (page 2, section 0023-0025), each said level embodied in said electronic test system as a software object (page 2, section 0023-0025).

Regarding claim 11:

Sutton discloses an electronic test system comprising an electronic processor (fig. 1, unit 102); an electronic memory coupled to said electronic processor (fig. 1, unit 101); a hierarchical structure residing in the memory and executed by said processor (page 2, section 0023-0025), said hierarchical structure having multiple levels (page 2, section 0023-0025), each level embodied in the electronic test system as a function defined by a class(page 2, section 0023-0025), wherein the implementation of the function is defined by the user of the

hierarchical structure by implementing the class (page 2, section 0026-0027, fig. 3, unit 313); said classes including a measurement class corresponding to a measurement to be performed on said device (fig. 3, unit 310, 312, 311), a test class corresponding to one or more related measurements (fig. 3, unit 310, 312, 311), and a procedure class corresponding to an ordered list of tests to be performed on said device (page 2, section 0023-0025).

Regarding claim 21:

Sutton discloses a method for producing an electronic test system software program for testing an electronic device under test (DUT), said program including a hierarchical structure having multiple levels including a measurement level corresponding to a measurement to be performed on said DUT (page 2, section 0023-0025), a test level corresponding to one or more of said measurements (page 2, section 0023-0025), and a procedure level corresponding to an ordered list of said tests to be performed on said DUT (page 2, section 0023-0025), each level embodied in said program as a software object for testing a device under test (DUT) (page 2, section 0023-0025), said method comprising the steps of providing a set of functions wherein the implementation of the functions is defined by said hierarchical structure (page 2, section 0023-0025); implementing the functions to define said test system software program (page 2, section 0023-0025, fig. 3, page 2, section 0021); generating said electronic test system software objects by implementing said functions (page 2, section 0023-0025); and utilizing said software objects to test said DUT (page 2, section 0021).

Regarding claim 23:

Sutton discloses a computer-readable medium on which is stored a program for testing an electronic device under test (DUT) (fig. 1, unit 108), said computer program comprising a measurement software object corresponding to a measurement to be performed on said DUT (page 2, section 0023-0025); a test software object defining a test algorithm utilizing parameters provided by said measurement object and corresponding to a test to be performed on said DUT (page 1, section 0021); a procedure software object corresponding to an ordered list of said tests to be performed on said DUT (page 2, section 0023-0025); and a plurality of software pointers linking said measurement object, said test object (page 2, section 0023-0025), and said procedure object (page 2, section 0023-0025, fig. 2, unit 206, 210).

Regarding claims 2, 4, 5, 8, 9, 10, 16, 18, 15, 7, 19, 22, 24, 12:

Sutton also disclose An electronic test system wherein said hierarchical program structure further includes a datapoint level corresponding to a single result of a measurement, and said measurement level includes a plurality of said datapoints (fig. 2, section 210, 211, 212); an electronic test system wherein said hierarchical program structure further includes a datapoint level, and said measurement level corresponds to a group of said datapoints, said datapoint level embodied in said electronic test system as a datapoint software object (fig. 2, unit 202, page 1-2, section 0021-0024); An electronic test system wherein said

hierarchical program structure further includes a product model level corresponding to a set of procedures for testing a family of said DUT (fig. 1, unit 117, 108); An electronic test system wherein said test object defines a test algorithm (page 2, section 0025). An electronic test system wherein said test algorithm comprises one or more electronic operations defined by software code, and the electronic parameters for said electronic functions are provided by said measurement Io object (page 2, section 0023-0025). An electronic system wherein said test object contains said measurement object, and said measurement object contains said datapoint object (fig. 2, unit 210). An electronic test system wherein said electronic processor further is adapted for electronically communicating with said DUT for executing said test software on said DUT and receiving a plurality of electronic outputs from said DUT corresponding to said measurement objects and said datapoint objects (fig. 2, unit 210). An electronic test system comprising plug-in software code components residing in said memory and providing an interface to other systems (fig. 1, unit 101); controlling temperature and humidity (page 1, section 0005); using COM file (page 2, section 0024); datapoint is subset of measurement level (fig. 2, section 206, 210), the class linked to measurement class (fig. 2, unit 206).

Claim Objections

2. Claims 6, 13, 14, 17, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitation of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: prior art fail to capable of beginning and ending the selected process, use of a touch pad, Active X Com interface, a second set of object methods for creating a test and procedure object containing test object, use of DLL file, use of ActiveX interface. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 RightFAX Telephone Numbers : TC2800 Official Before-Final RightFAX - (703) 872-9318, TC2800 Official After-Final RightFAX - (703) 872-9319

TC2800 Customer Service RightFAX - (703) 872-9317

BRYAN BUI
PRIMARY EXAMINER